EXHIBIT 11

EXHIBIT 2

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. NXP SEMICONDUCTORS N.V., et al..	Case No. 7:24-cv-00028-DC-DTG

PLAINTIFF'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

I. Introduction

U.S. Patent No. 8,549,339 (the "'339 Patent") teaches an innovative multi-core processor with sets of processor cores. In particular, the '339 Patent teaches various means of coordinating not just the individual cores of the multi-core processor but the sets of processor cores that operate as a unit. While previous techniques focused on coordination among individual cores, the '339 Patent focuses on coordination as to sets of cores.

Defendant's arguments ignore this focus. Despite agreeing that "set of processor cores" means a "group of two or more processor cores," Defendant fails to apply this definition properly. Instead, Defendant reads a disavowal of any single-reference-oscillator architecture, where the Applicant explains how the prior art does not teach *sets* of processor cores. Both references only teach sending a single, unprocessed clock signal to anything that could be considered a "set" of processors. The Applicant explained as much. Thus, Defendant's purported "word-for-word" construction is drawn from disparate descriptions of the prior art to create a limitation the applicant never intended.

Defendant's indefiniteness arguments fare no better. First, a POSITA would readily understand the meaning of "configure[] to dynamically receive." Second, the term "periphery" has sufficient meaning and is not a term of degree. Third, the phrase "a common region that is substantially central" is well-disclosed by the specification.

II. Disputed Terms Requiring Construction

a. Term 1: "the first clock signal is independent from the second clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Plain and ordinary, meaning, where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks**

The claim term "the first clock signal is independent from the second clock signal" is straightforward and does not require additional construction beyond its plain and ordinary meaning. Defendant, however, proposes an unnecessary and restrictive construction which contradicts both the plain meaning of the term and the prosecution history. Defendant's "word-for-word" construction is nowhere to be found in the prosecution history. Instead, the applicant made it clear that the use of "independent" is best understood as simply meaning "different." Defendant draws its flawed construction from a misunderstanding of both the claim language and the prior art.

During prosecution, the applicant amended the claims to clarify the relationship between the clock signals and the PLLs, specifying that the first and second clock signals are inputs to separate PLLs associated with different sets of processor cores. The examiner initially rejected claims reciting "a first set of processor cores … configured to dynamically receive … a first clock signal; a second set of processor cores … configured to dynamically receive … a second clock

signal," in view of Jacobowitz and Kim[1]. Dkt. No. 39-7. In response, the applicant made several amendments including to add the disputed term. Notably, however, the first and second clock signals of the original claim are not the same signals as in the disputed term. Rather, the original first and second clock signals became the first and second *output* clock signals of the first and second PLLs while the new first and second clock signals of the disputed term are the *inputs* to the PLLs. Dkt. 39-9 at 3.

Original Claim Language	Amended Language
1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each dynamically receive a first supply voltage and a first clock signal; A second set of processor cores of the multi-core processor, wherein each processor core form the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input; A second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

[1] Jacobowitz refers to U.S. Publication No. 2009/0106576 (Dkt. No. 39-5). Kim refers to U.S. Publication No. 2009/0138737 (Dkt. No. 39-6).

Put in terms of Figure 3 from the specification, the clock signal of the original claim referred to the arrow entering Core 152 while the clock signal of the disputed term refers to Clock Signal 1, 2, and/or 3. *See* Dkt. No. 39-8 ("However, the broadest reasonable interpretation of the recited claim language (i.e., claim 1: first set of processor cores configured to dynamically receive a first clock signal) reads on the clock output of the local oscillators of Jacobowitz and also reads on the output of the PLLs shown in applicant's figure 3.") In terms of Jacobowitz[2], the original clock signal was V_0 or V_1 while the clock signals of the disputed terms refer to V_R:

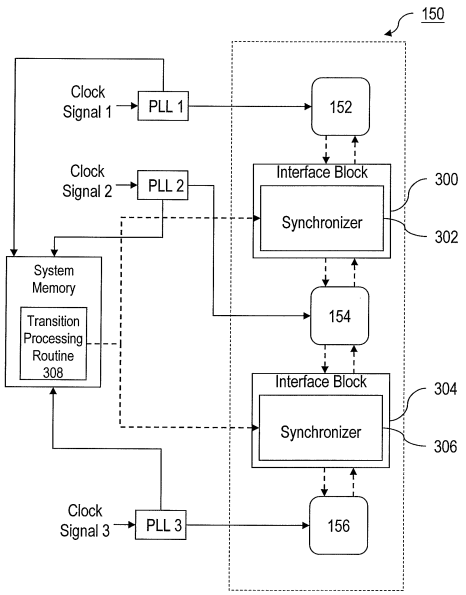

FIG. 3

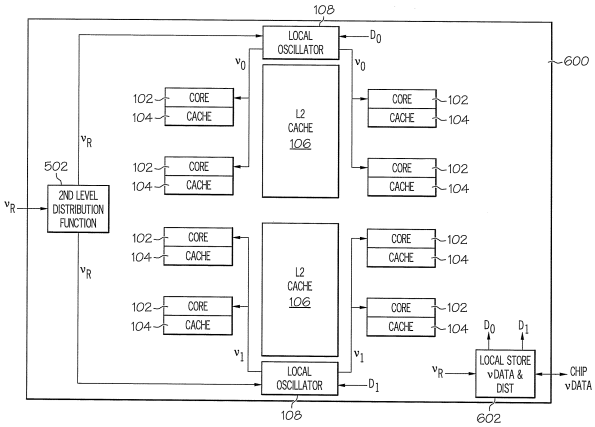

FIG. 6

'339 Patent at Figure 3; Jacobowitz at Figure 3. Because there was no distinction in the claim between the input and output signals of the PLLs, at least under the broadest reasonable interpretation, the examiner rejected any distinction that Clock Signal 1, 2, 3 were "different/independent" while V_R was only a single signal. Dkt. No. 39-8.

[2] Jacobowitz, of course, does not teach the claims and thus mapping the claimed terms to Jacobowitz is of only limited illustrative value.

Nowhere during prosecution did Applicant ever clearly disavow a single clock system, as Defendant contends. Applicant's remarks were focused on the clock signal as an *input*. Dkt. No. 39-9 at. 9-10 ("Jacobowitz clearly show[s] that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (V_R) and distributes V_R to local oscillators 108. [] Jacobowitz fails to disclose or teach … a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input, respectively." (emphasis in original)). As to Kim, the applicant did not even argue independence of the signals was distinguishing, merely acknowledging it as a limitation. *See Id*. at 10 ("In addition , Kim also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal.")

What the Applicant did describe was the absence of any "set of processor cores" in either Jacobowitz or Kim. That is the first and most important distinction over both pieces of prior art—not a single clock system. The Applicant explained that, while Jacobowitz mentions that "[f]urther power management can be realized by controlling supply voltage (Vdd) to each core and/or chip," this statement does not provide any reference to "sets of processor cores"—only to individual cores. *Id*. at 9. Likewise for Kim, the applicant explained: "Kim discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4})." *Id*. at 10. This *was* clear disavowal, and Plaintiff and Defendant accordingly have agreed to a construction of "set of processor cores."

Despite Defendant failing to demonstrate any clear disavowal as to "independent," it nonetheless still contends that construing the disputed term is necessary to avoid permitting the claims to cover the "exact arrangement" of Jacobowitz and Kim. Dkt. No. 39 at 10. However, neither reference teaches the "arrangement" supposedly motivating Defendant's proposed construction. In particular, there is no basis to insert the phrase "or processed (i.e. divided or multiplied) from a single reference oscillator clock." No prior art considered in the prosecution teaches providing such a first and second clock signals to a respective first and second PLLs associated with a first and second set of processor cores. First, Jacobowitz does not discuss processing the signal of the reference clock before reaching the first and second PLLs. Instead Jacobowitz provides the unprocessed signal directly to the Local Oscillators. *See* Jacobowitz at ¶¶ [0037] - [0038]. In contrast, while Kim does teach processing a single reference oscillator clock with a main PLL having multiple frequency dividers prior to reaching further PLLs, only the main PLL is taught to be associated with multiple cores. Kim at ¶ [0024]. Kim does not teach providing processed signals from a single clock source to multiple sets of processor cores as claimed. Defendant's construction does not prevent "recapture" of any considered prior art.

Defendant's further discussion of "multiple and independent" is also unavailing. Even if "independent" is not coextensive with "multiple," it does not follow that "independent" must mean "provided by or processed (i.e., divided or multiplied) from [different] reference oscillator clocks." This logical leap has no basis in the prosecution history. Defendant ignores that the only occasion the Applicant used the phrase "multiple and independent" was in reference to the "resuming communications" limitation of claims 15 and 18 not claim 1. Dkt. No. 39-9 at 11. In any case the Applicant also reemphasized that neither Jacobowitz nor Kim teach "sets of processor cores." Dkt. No. 39-9 at 11. The Applicant explained neither reference "discloses having *sets* of processor cores

configured to receive multiple and independent clock signals." *Id*. (emphasis added). As Kim does not have sets of processor cores at all and is the only source for the "processed (i.e., divided or multiplied)" language, finding a clear disavowal here is improper.

If the Court finds that "independent" needs clarification—it does not—it merely means "different." This is the term that the applicant used interchangeably with "independent" and is what the examiner clearly understood it to mean. *See* Dkt. No. 39-8 ("Applicant's representative referred to figure 3 of the specification and stated that clock signals 1 through 3 were different/independent clock signals input to the PLLs…"(emphasis added)). Defendant's attempt to redefine "independent" is inconsistent with both the applicant's amendments and examiner's understanding.

b. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Indefinite**[3]

Defendant argues because "configured to dynamically receive" does not have a common understanding in the field and "dynamically" is "vague," the disputed term is indefinite. This argument is unfounded.

First, the phrase "configured to dynamically receive" is plainly understandable to a POSITA. Both the advantages and difficulties of dynamically providing voltage and clock signals

[3] Plaintiff notes that while Defendant MediaTek and Defendant NXP argue the next three terms are indefinite and make similar arguments, the arguments are not identical and are supported by different experts.